VLSI Design Basics

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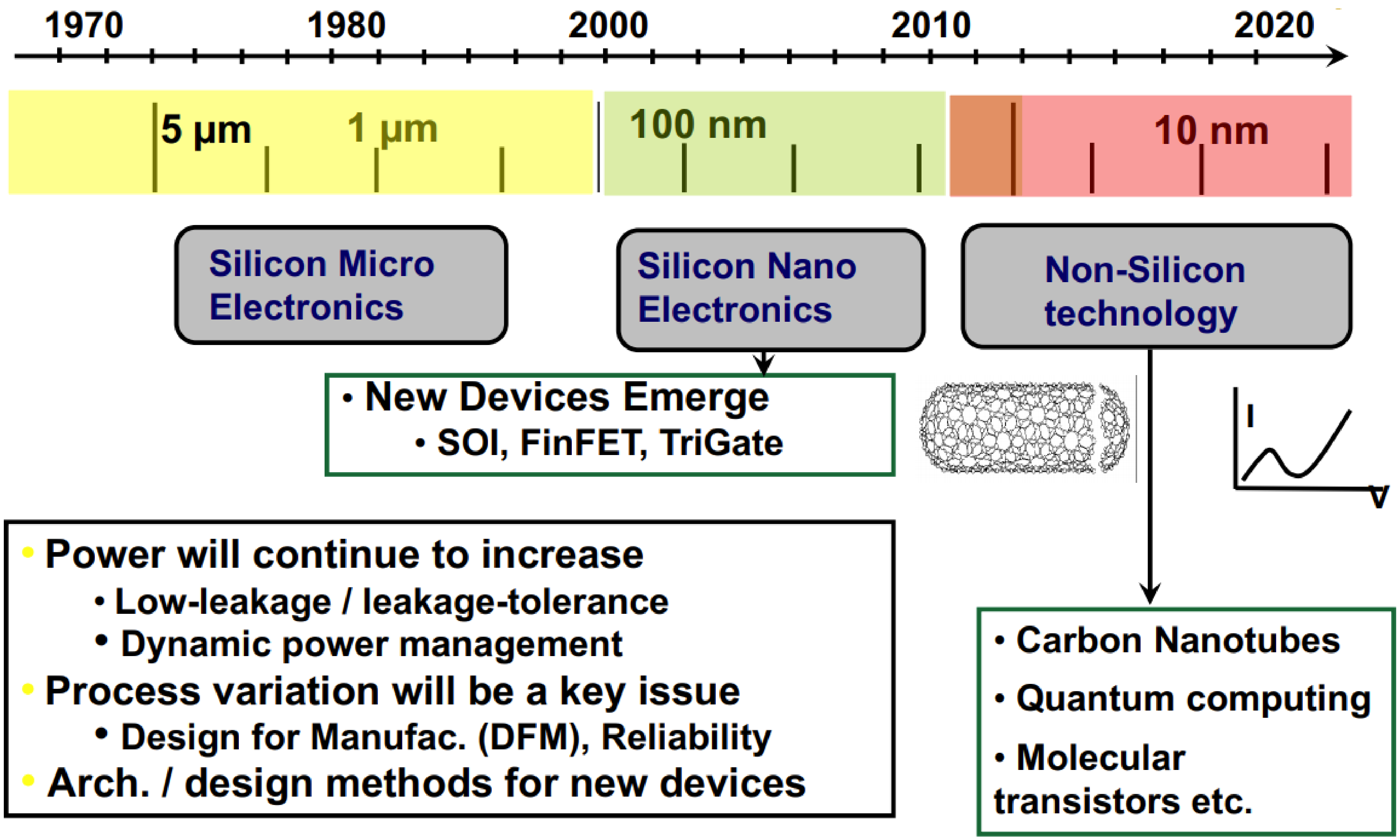
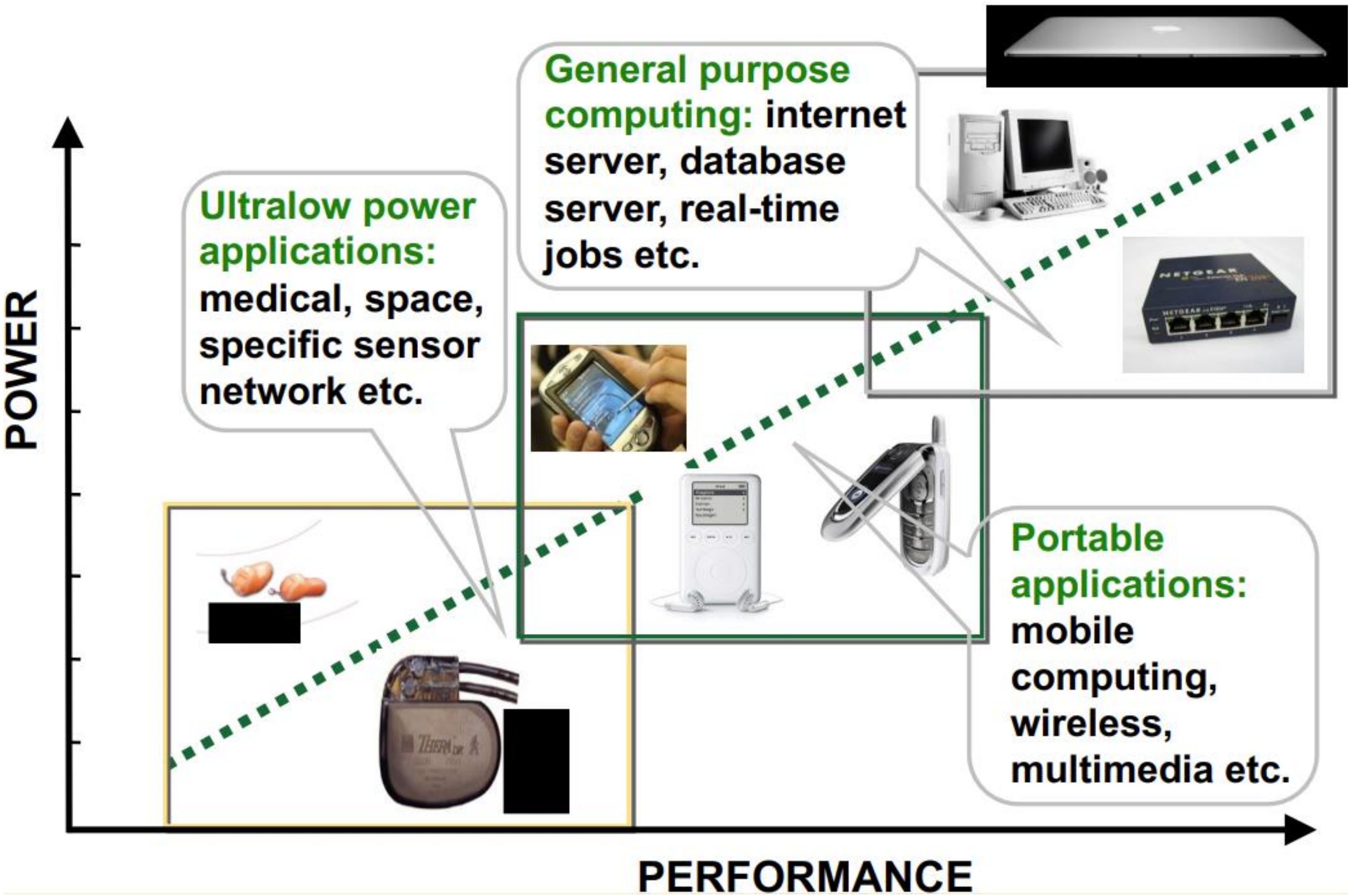
ELE594 – Special Topic on Hardware Security & Trust

University of Rhode Island

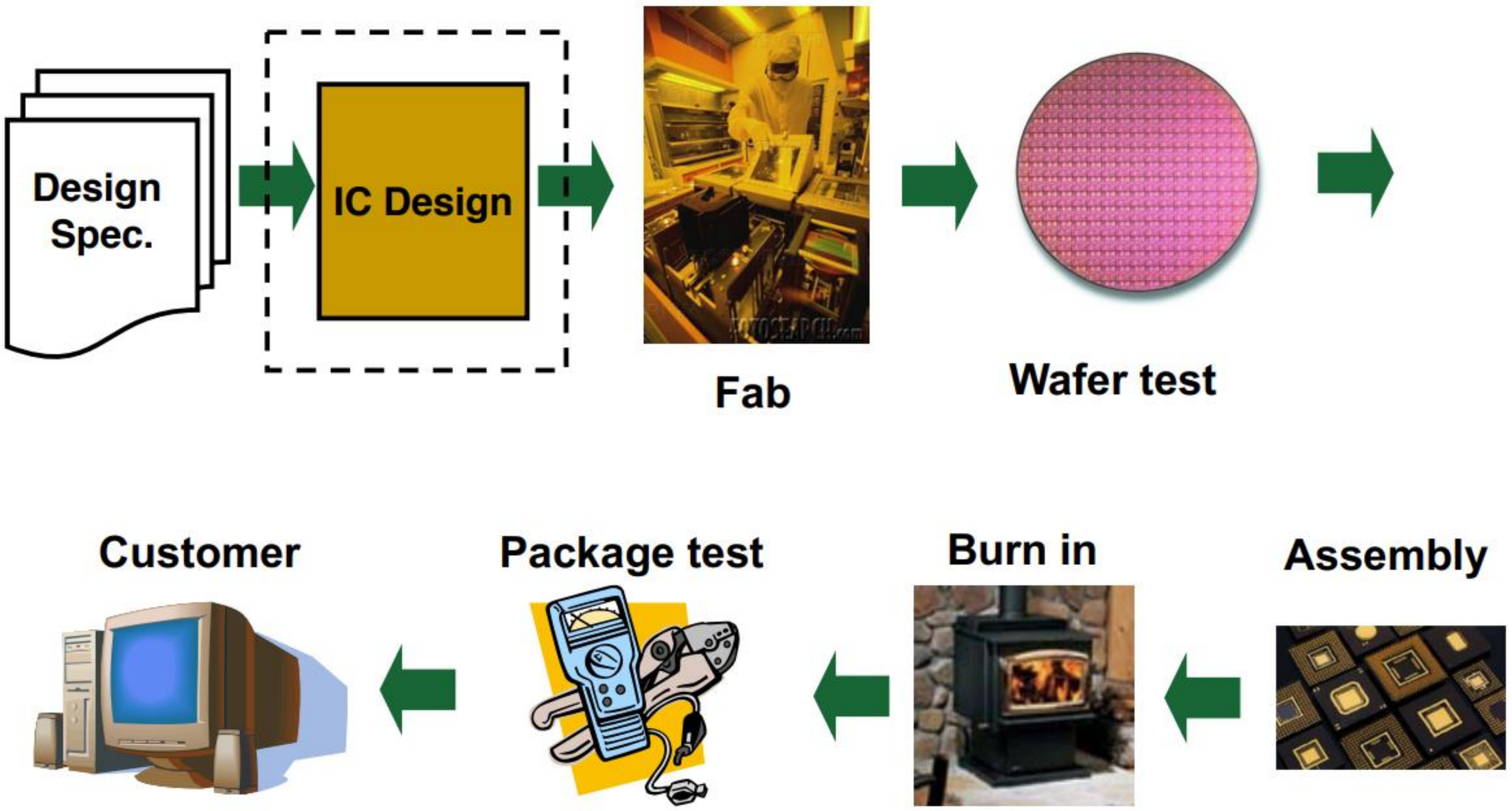
Semiconductor Roadmap



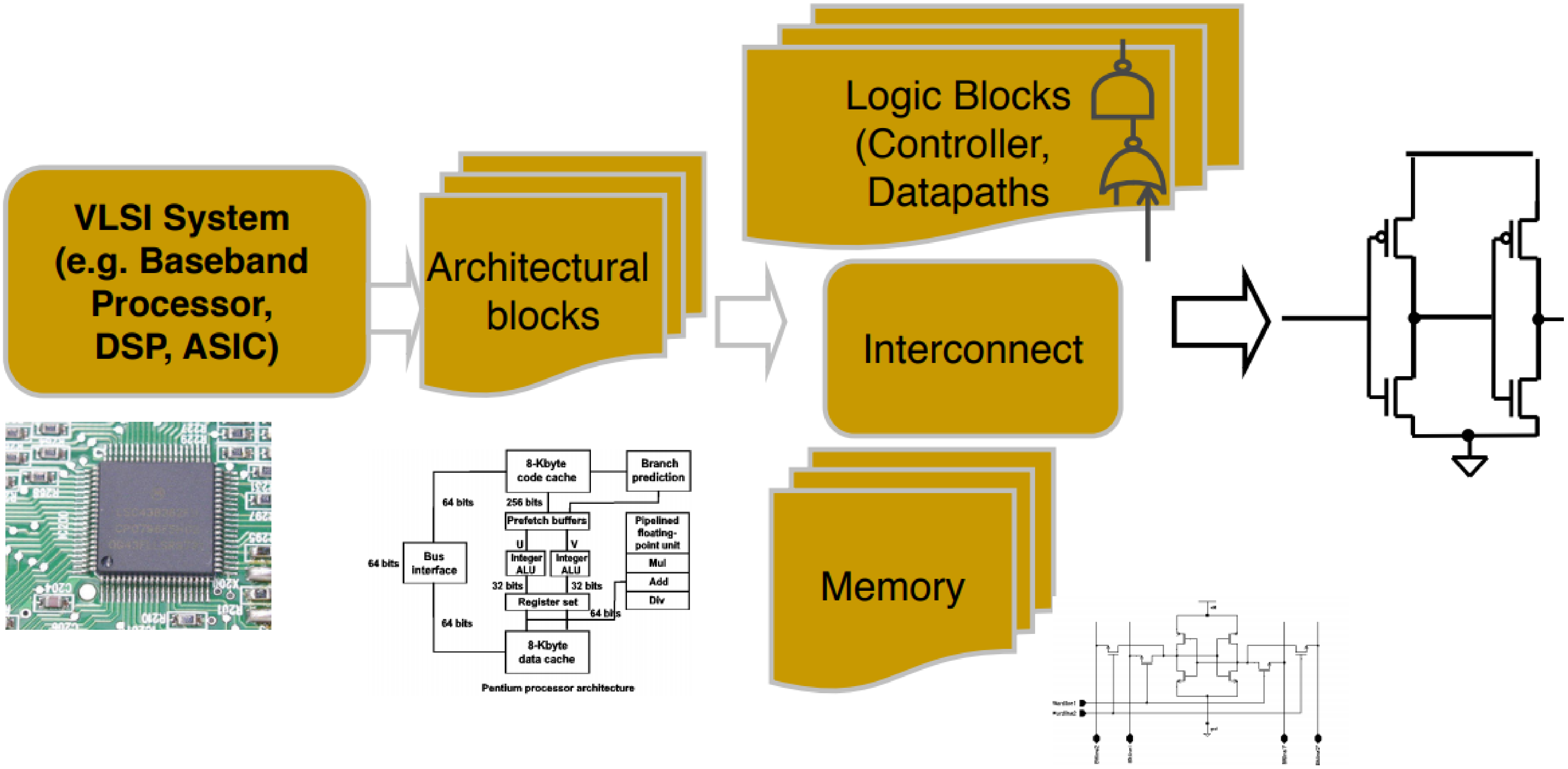
VLSI Applications



VLSI Design Flow

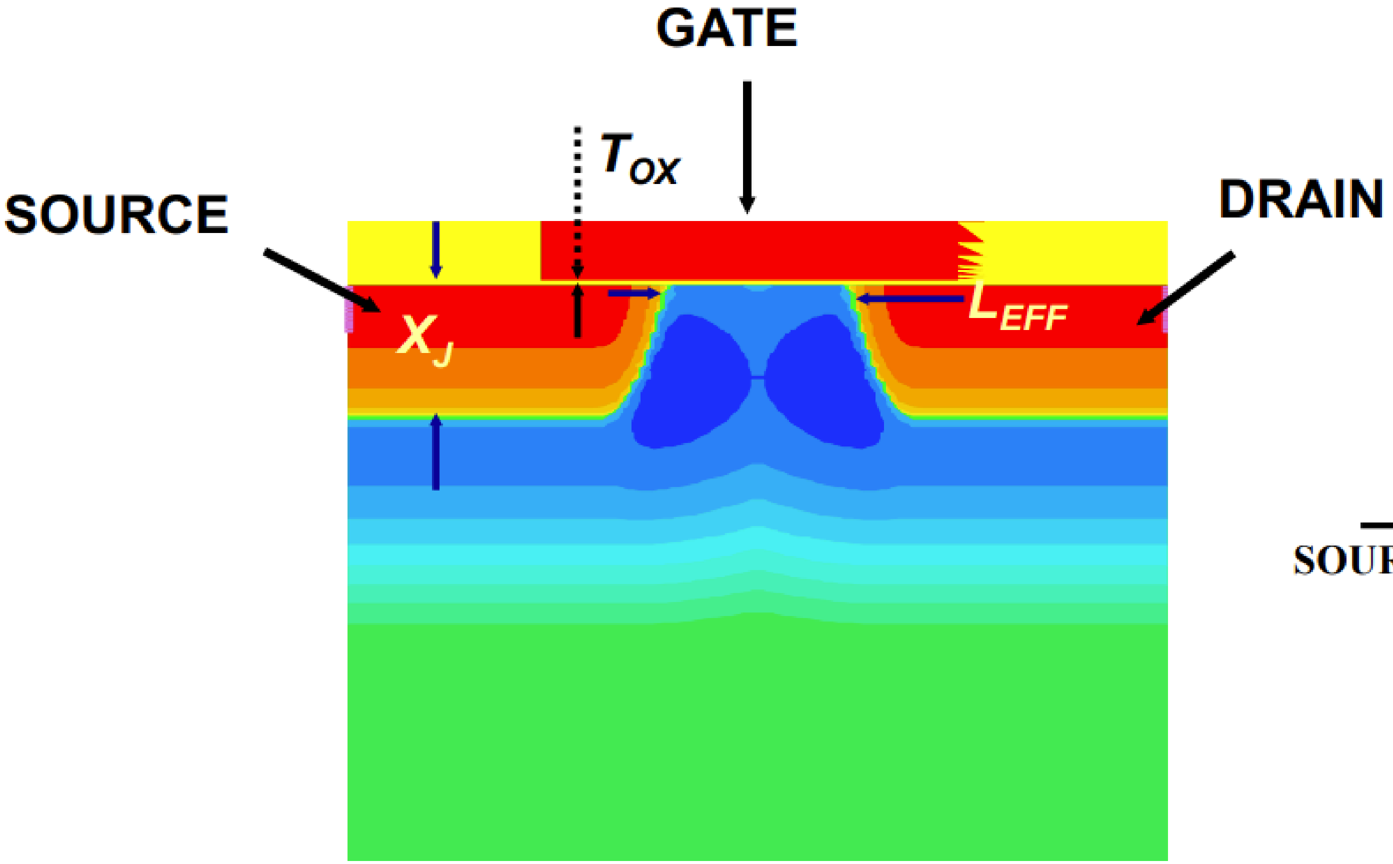


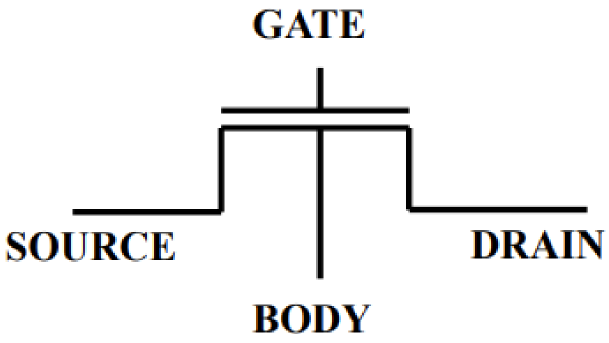
VLSI System Breakdown



System -> Architecture -> Logic ->Transistor

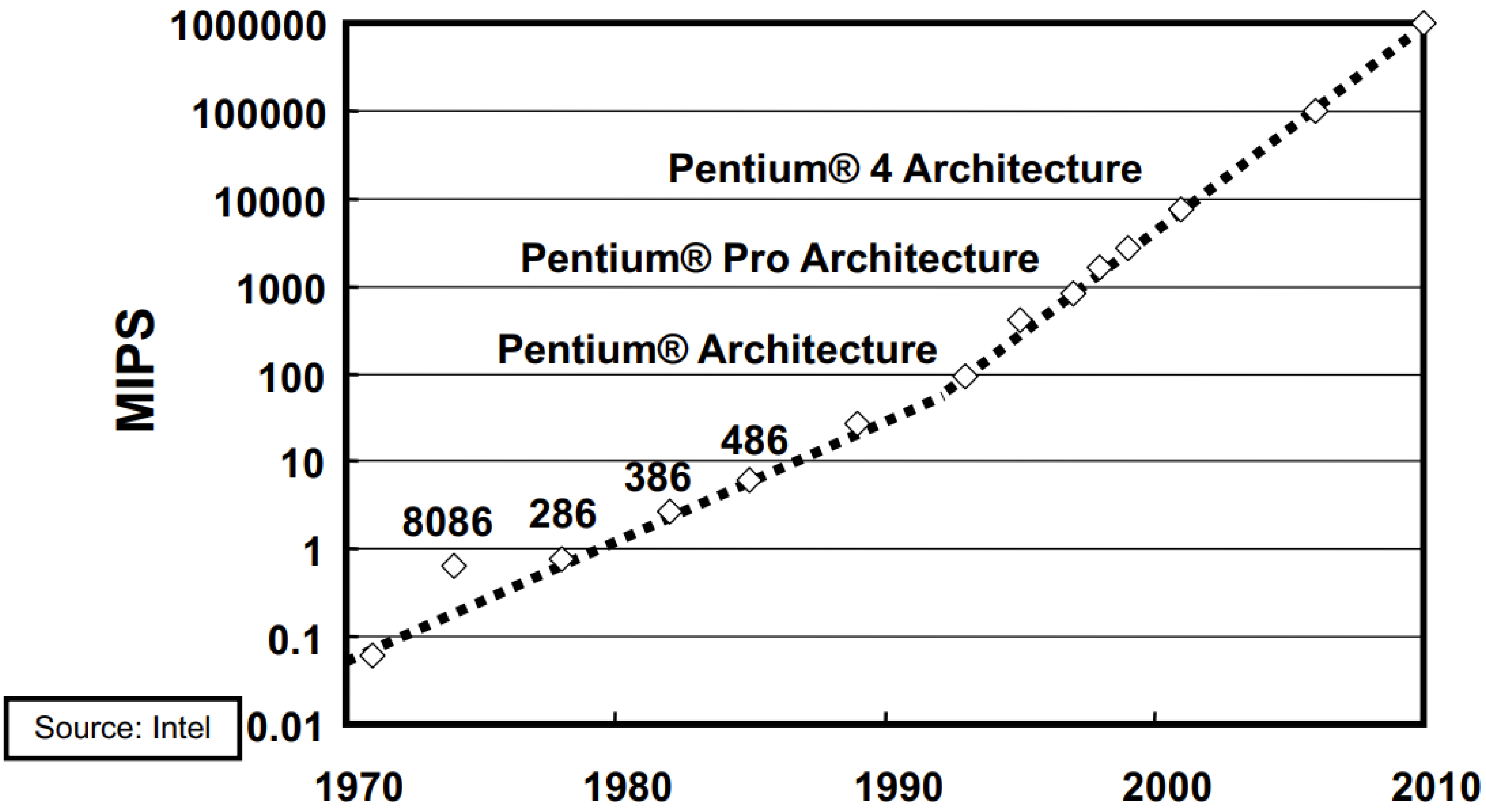
Transistor





- Underlying building unit for integrated circuit, e.g. logic gates and memory units
- Advanced commercial technology nowadays goes beyond 7 nm

Growth in Computing Power



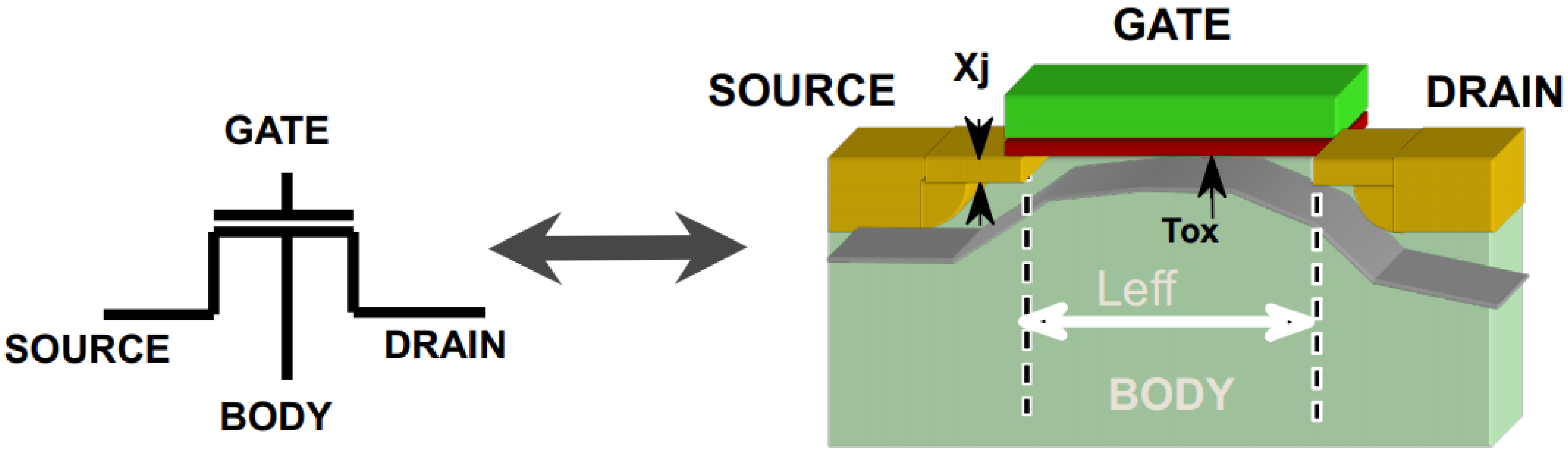
Moore's Law

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. ..."

***Electronics Magazine,* 19 April 1965**

	Year of Introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,180,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	24,000,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2002	220,000,000
Intel® Itanium® 2 processor	2003	410,000,000

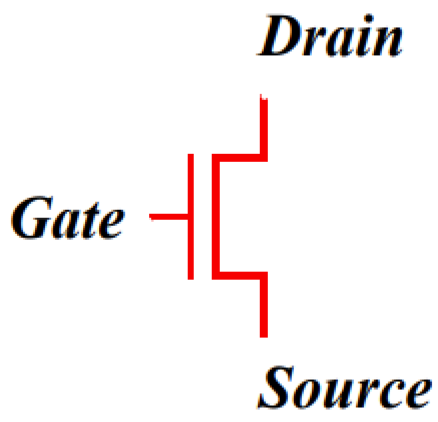
Technology Scaling

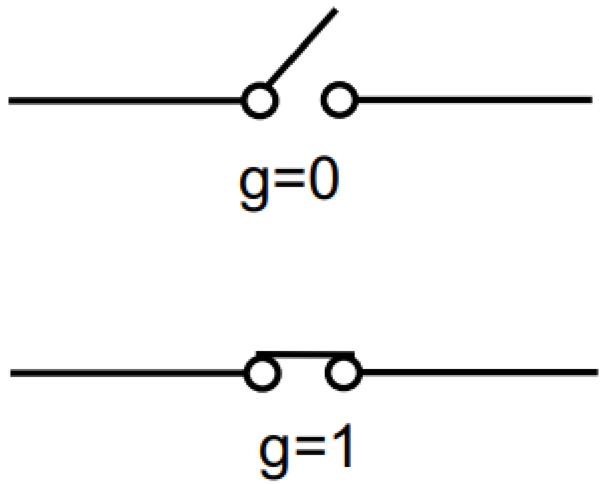


Dimensions scale down by 30%	Doubles transistor density
Oxide thickness scales down	Faster transistor, higher performance
Vdd & Vt scaling	Lower active power

N-type MOS Transistor

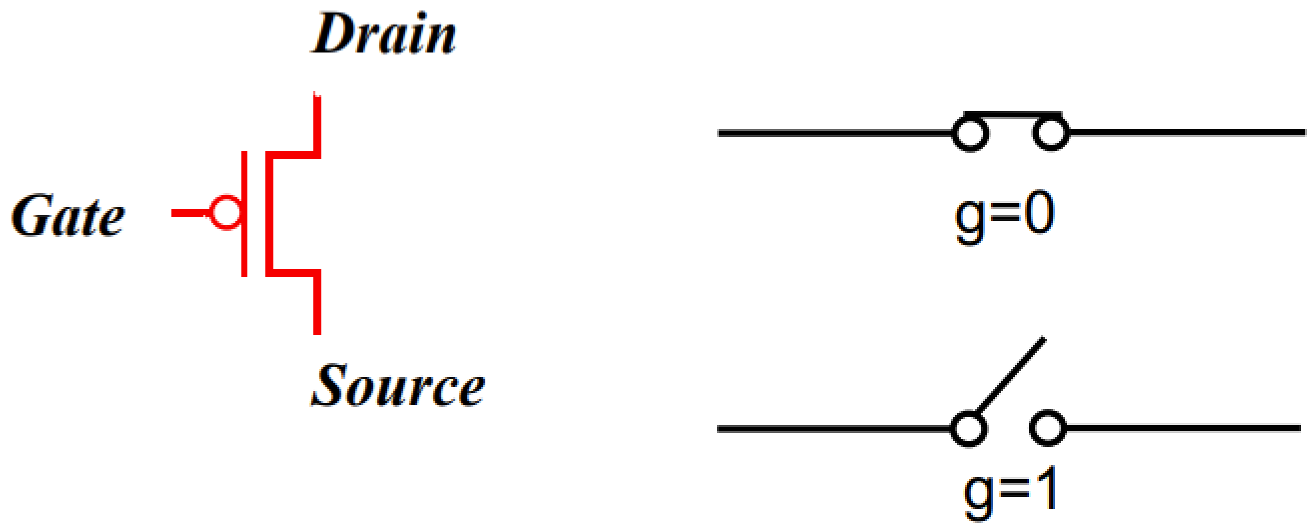
- If the gate is “high”, the switch is on
- If the gate is “low”, the switch is off



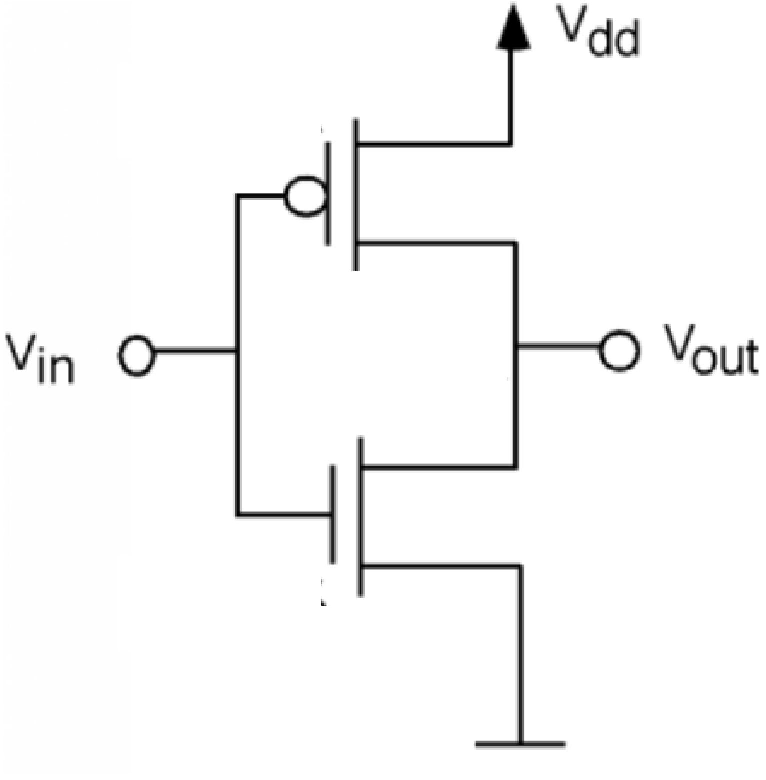


P-type MOS Transistor

- If the gate is “low”, the switch is on
- If the gate is “high”, the switch is off

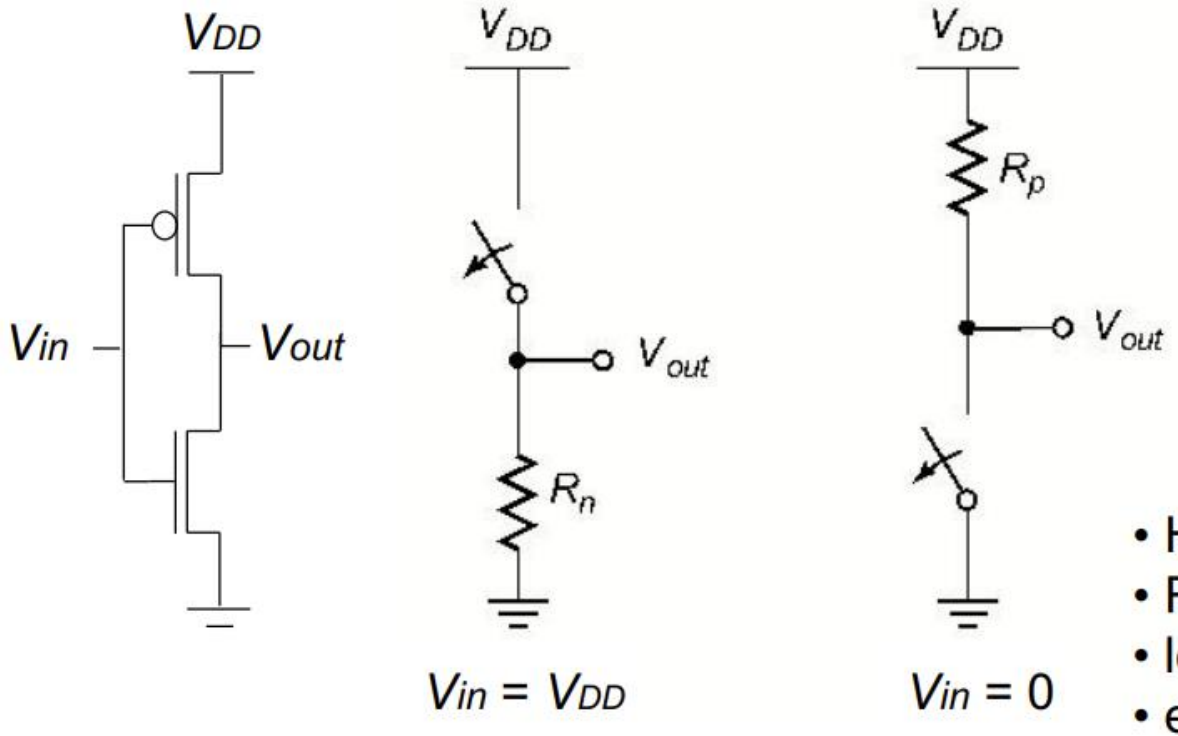


CMOS



- No static current flow
- Less current means less power

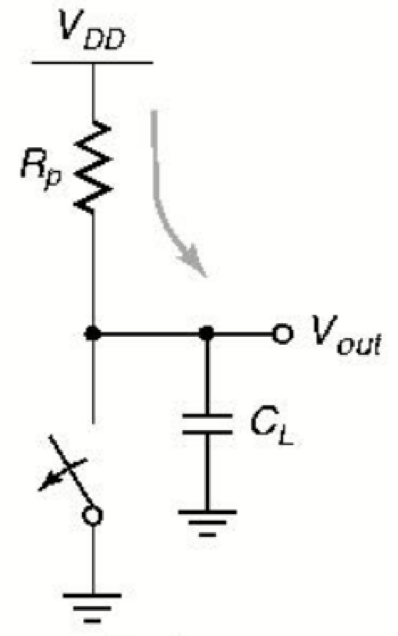
CMOS Inverter Analysis

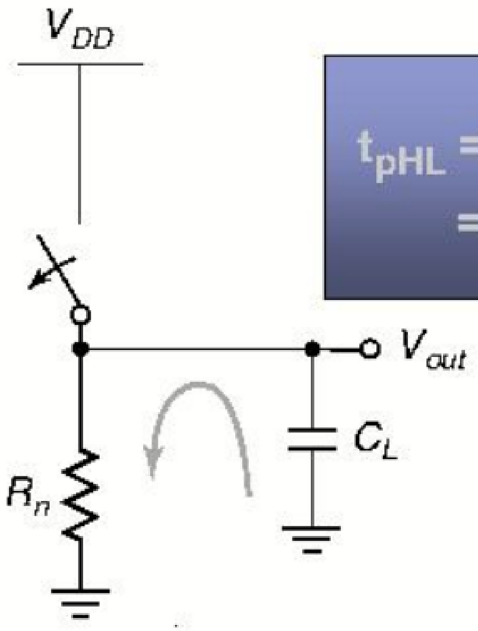


$V_{OL} = 0$
$V_{OH} = V_{DD}$

- High noise margin
- Ratioless
- low output impedance
- extremely high input impedance
- no static power

CMOS Inverter Analysis





$$t_{pHL} = f(R_{on}.C_L)$$
$$= 0.69\ R_{on}C_L$$

To reduce delay:

- Reduce CL
- Reduce Rp,n
- Increase W/L ratio

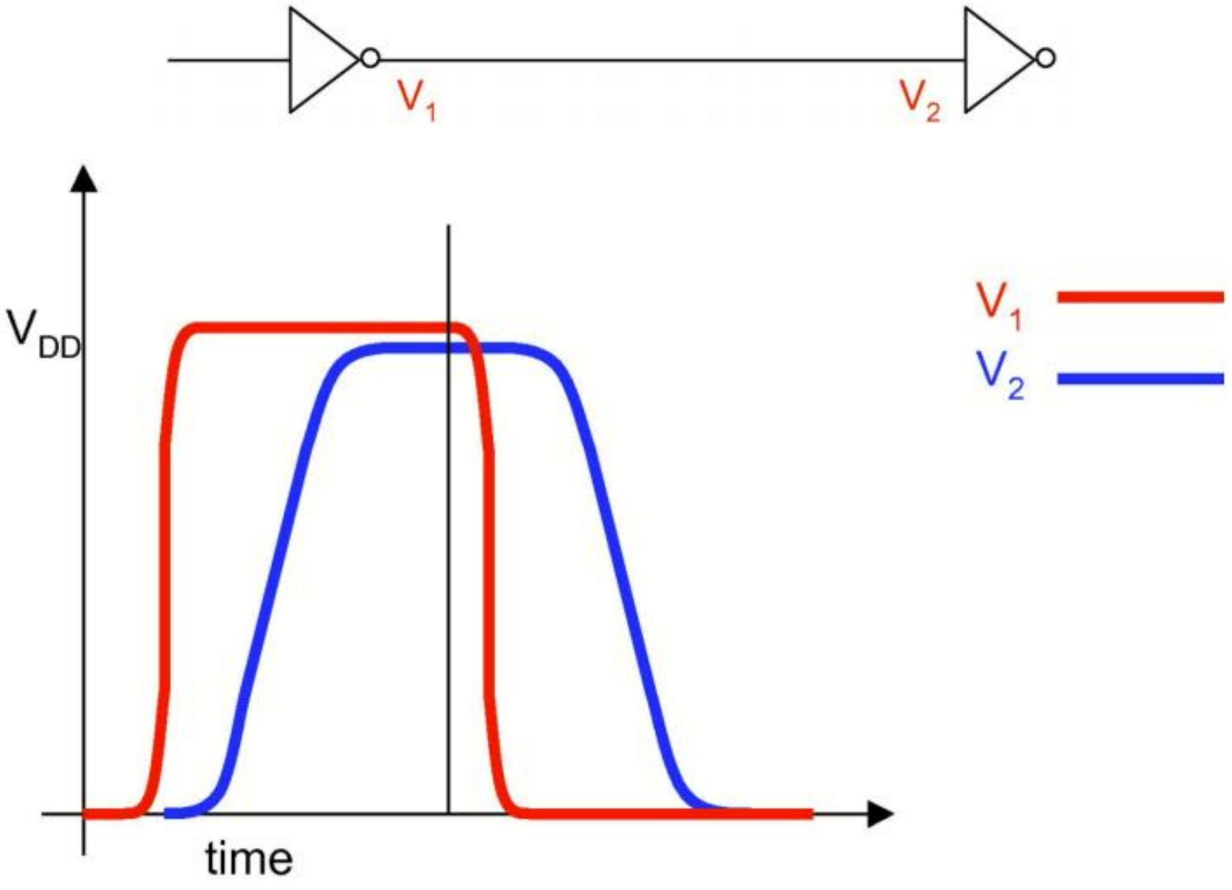
$V_{in} = V_{DD} \rightarrow 0$ $\qquad$ $V_{in} = 0 \rightarrow V_{DD}$

Output: Low-to-High $\qquad$ High-to-Low

CL is composed of the drain diffusion capacitances of the NMOS and PMOS transistors, the capacitance of connecting wires, and the input capacitance of the fan-out gates

CMOS Inverter Results

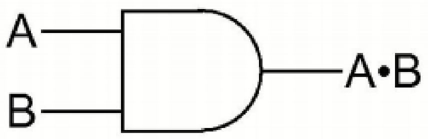
- Interconnect delay



Boolean Logic

- Basic operators
  - AND

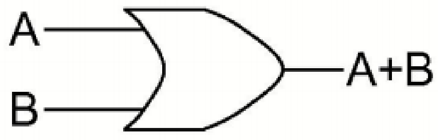
$$f(A,B) = A \cdot B = A \cap B$$



A	B	A•B
0	0	0
0	1	0
1	0	0
1	1	1

  - OR

$$f(A,B) = A + B = A \cup B$$

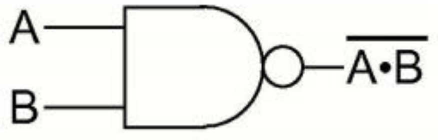


A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Boolean Logic

- Basic operators
  - NAND

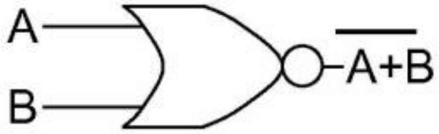
$$f(A,B)=\overline{A\cdot B}=\overline{A\cap B}$$



A	B	$\overline{A\bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0

  - NOR

$$f(A,B)=\overline{A+B}=\overline{A\cup B}$$



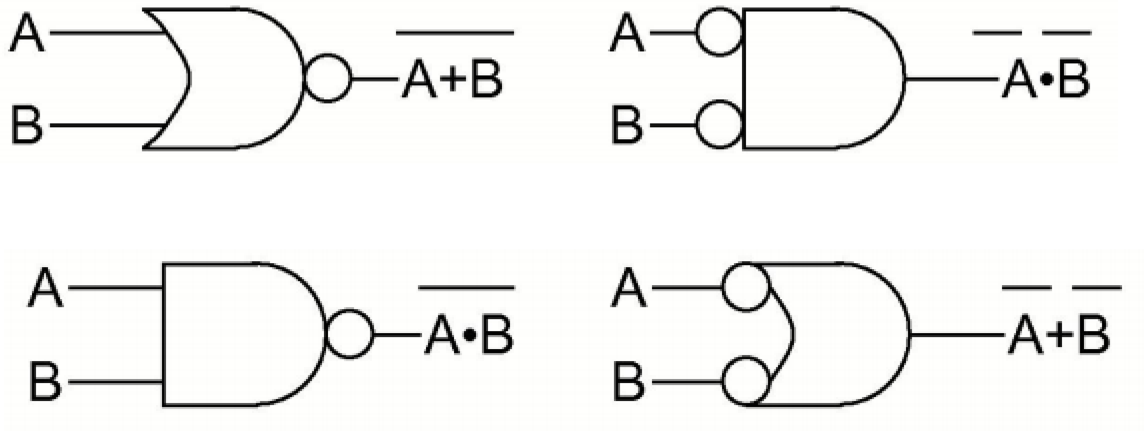
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Boolean Logic

- DeMorgan's Theorem

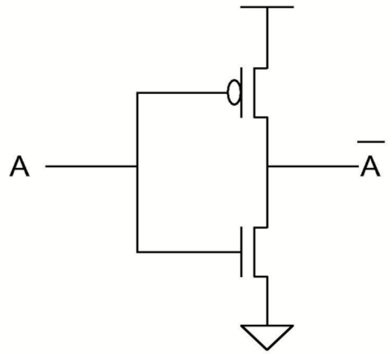
$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

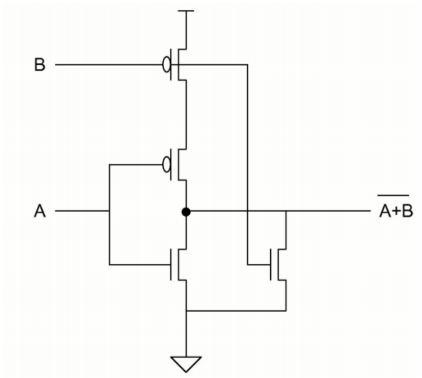


CMOS Logic Implementation

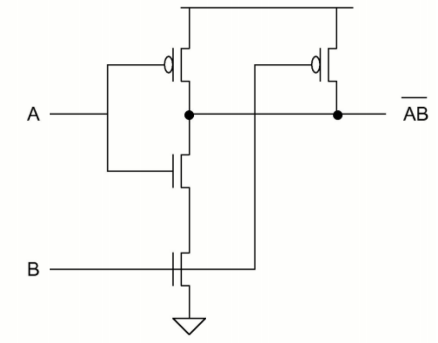
- Inverter



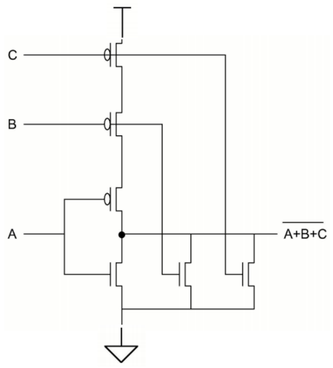
- NOR



- NAND

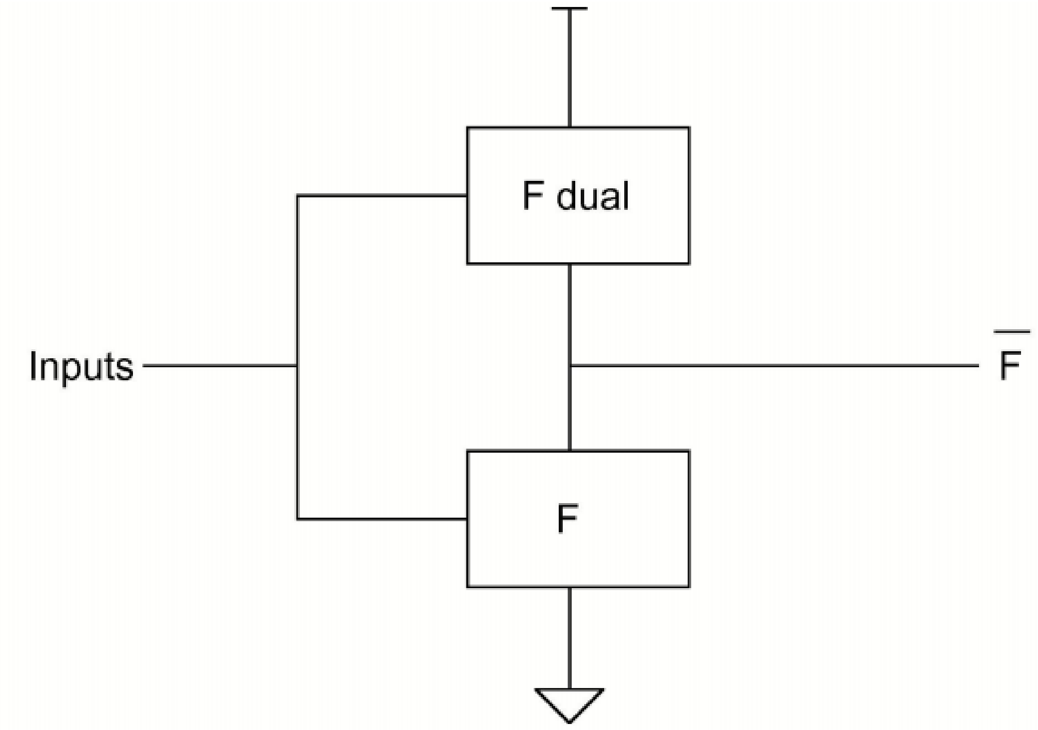


- Multi-input NOR



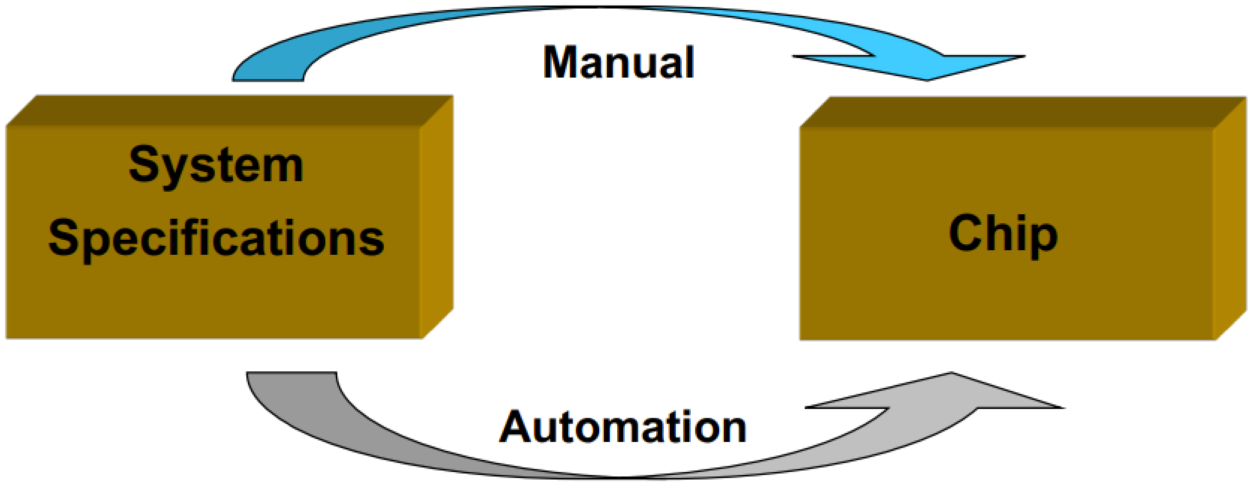
CMOS Logic Implementation

- General CMOS combinational logic

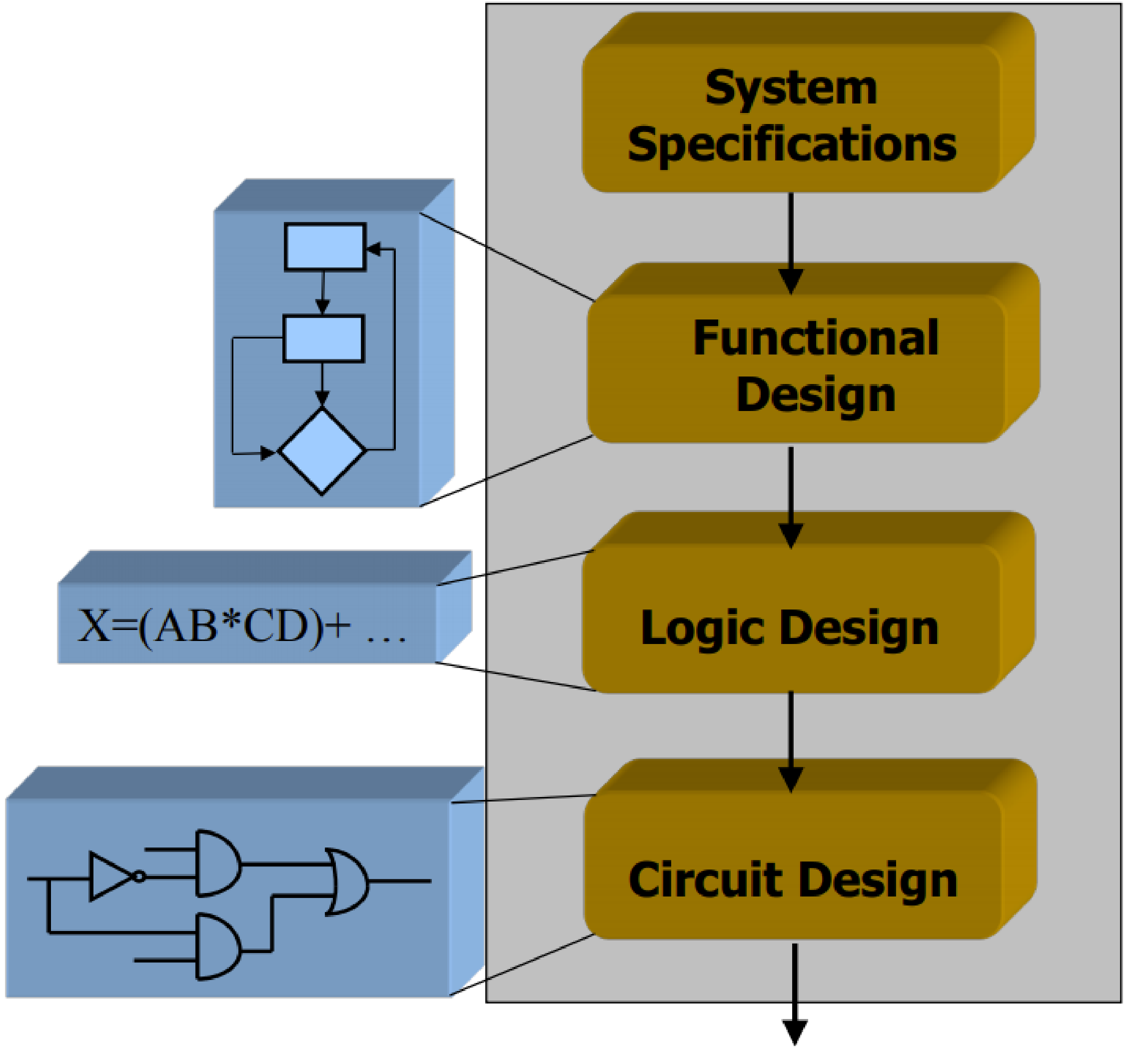


VLSI Design Flow

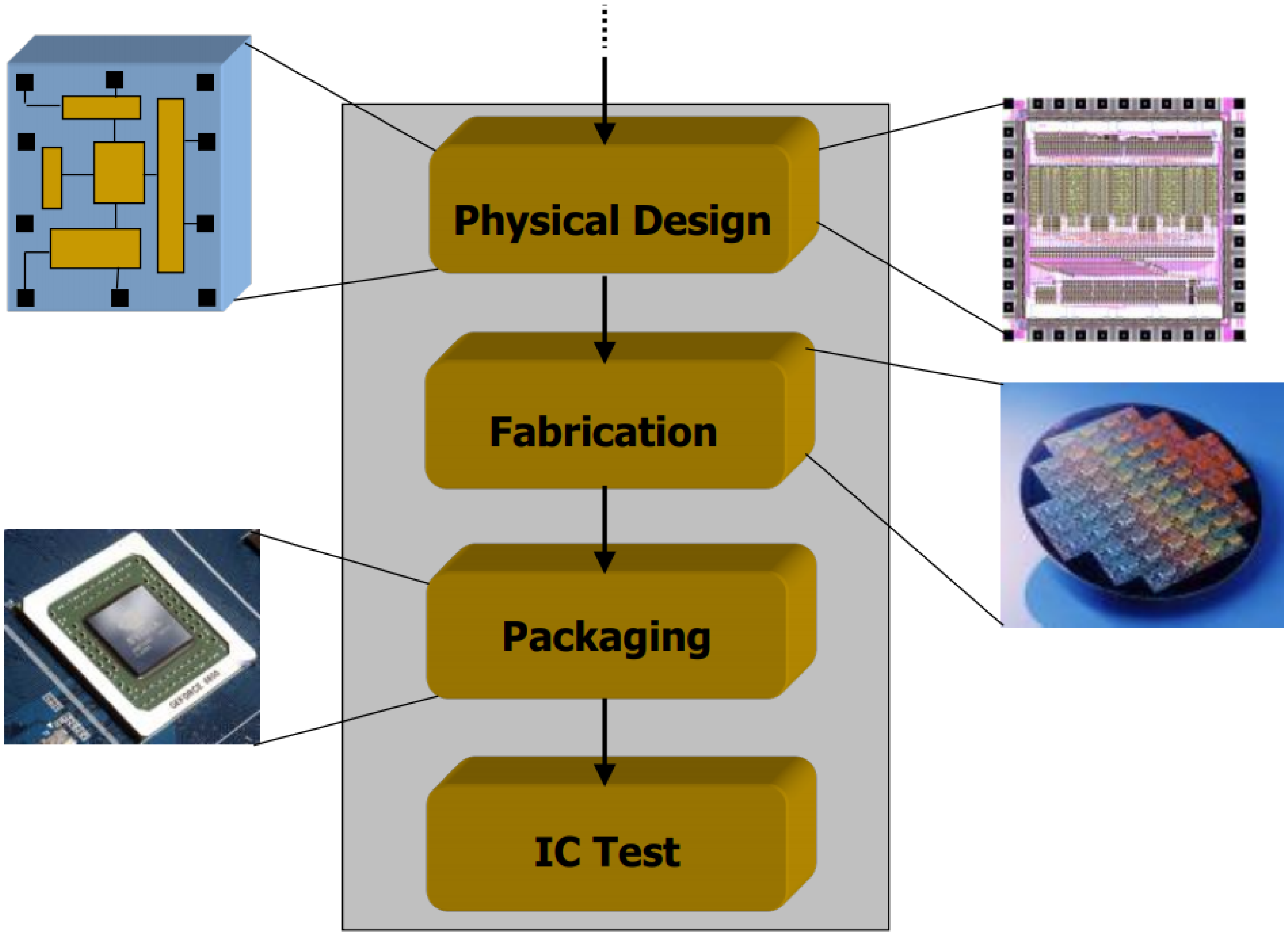
- Large number of components
- Optimize requirements for higher performance
  - Performance relates to speed, power and size.
- Time to market competition
- Cost
  - Using computer makes it cheaper by reducing time-to-market.



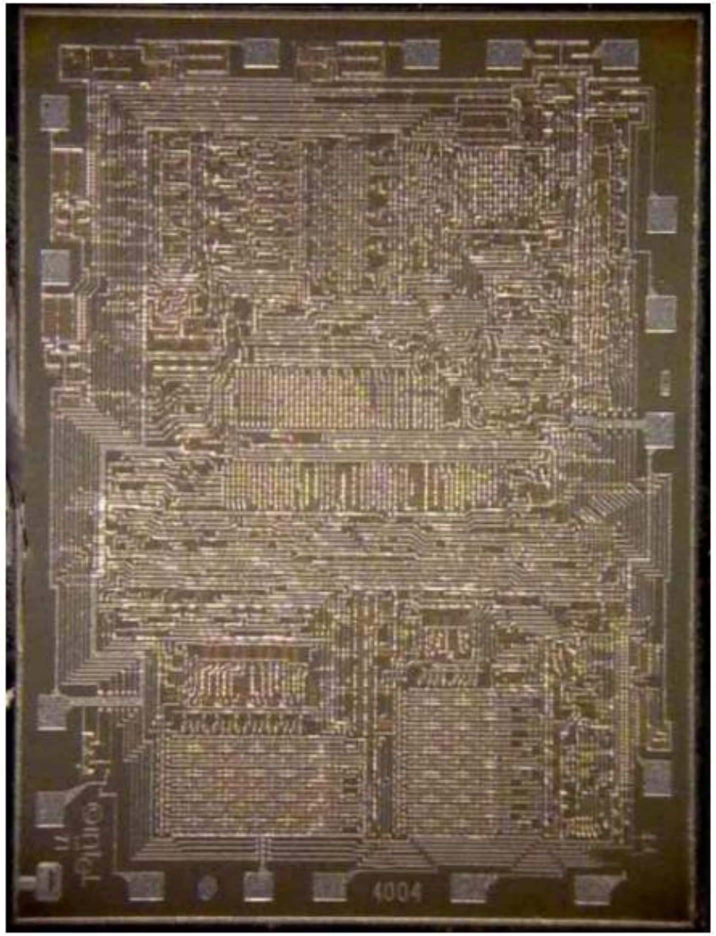
VLSI Design Flow



VLSI Design Flow

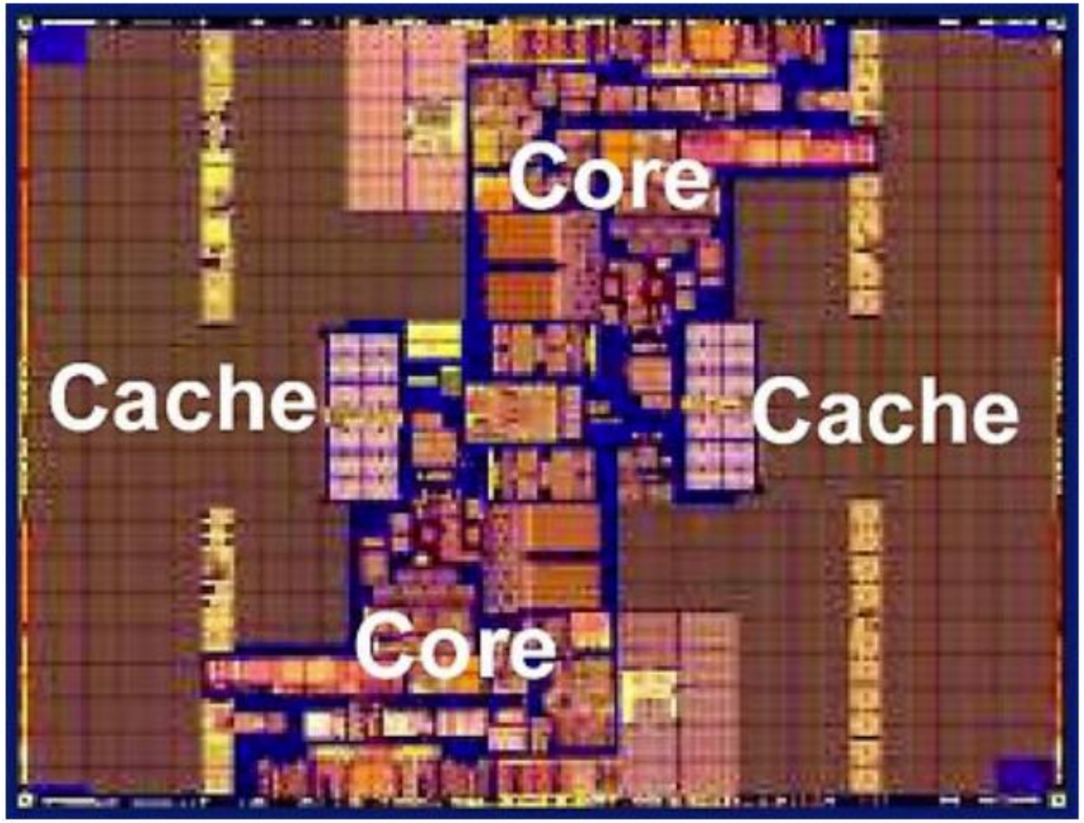


Intel 4004



- First microprocessor
- Designed in 1971
- 2300 transistors
- 10-um process
- ~100 KHz

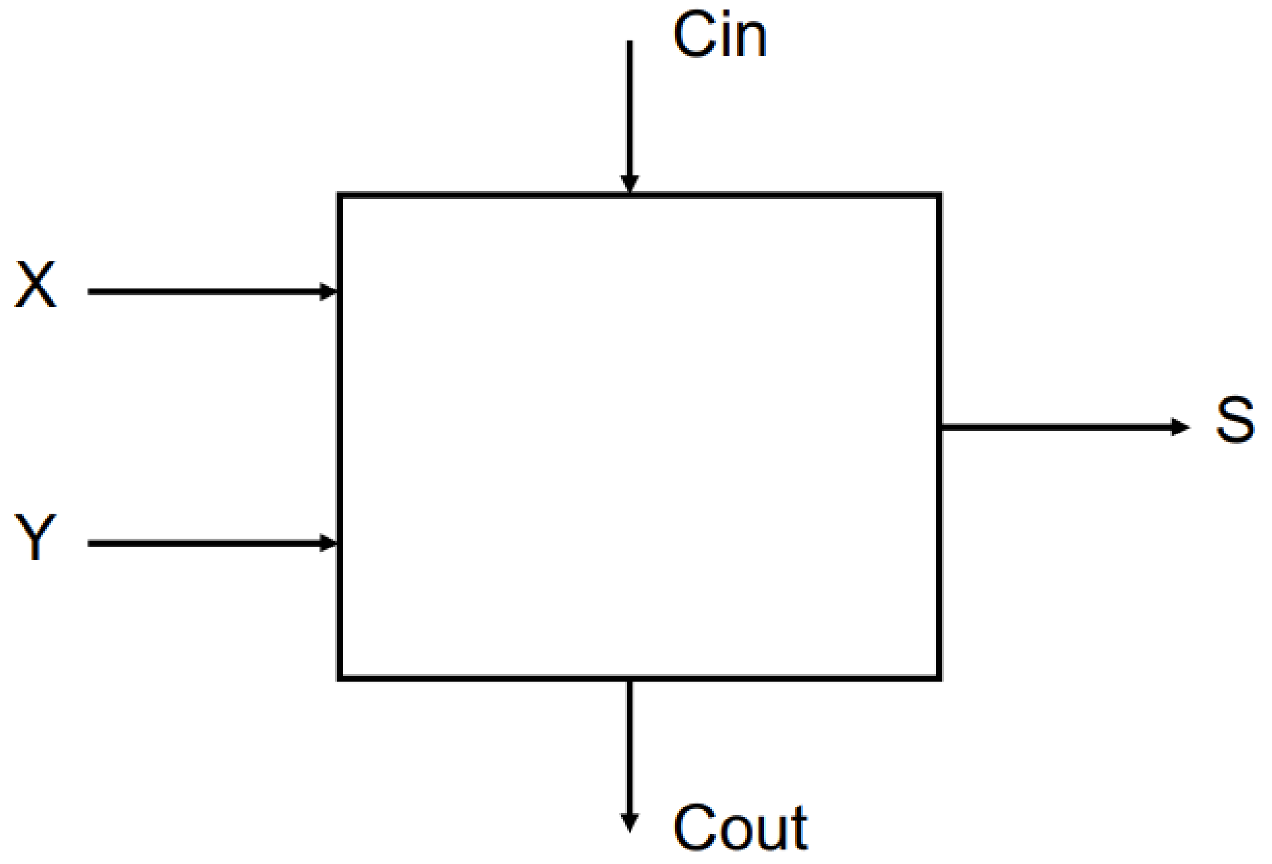
Intel Itanium Processor



- Released in 2005
- 1.72 Billion transistors
- 90-nm process
- 2 GHz

Functional Specification

- Full adder



Behavioral Specification

- VHDL
- Verilog

```
entity adder is
        -- i0, i1 and the carry-in ci are inputs of the adder.
        -- s is the sum output, co is the carry-out.
        port (i0, i1 : in bit; ci : in bit; s : out bit; co : out bit);
 end adder;
 architecture rtl of adder is
        begin -- This full-adder architecture contains two concurrent assignment.
         -- Compute the sum. s <= i0 xor i1 xor ci;
        -- Compute the carry. co <= (i0 and i1) or (i0 and ci) or (i1 and ci);

end rtl;
```

Behavioral Specification

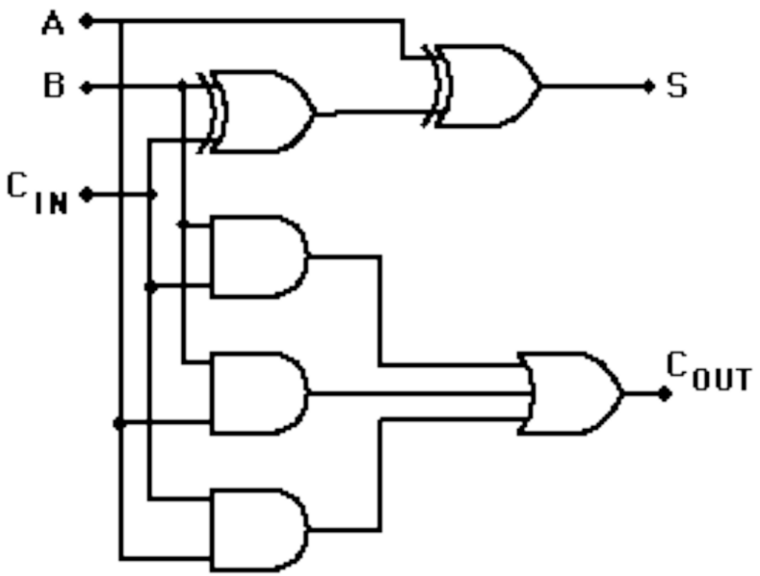
```
module fulladder (a,b,cin,sum,cout);
    input a,b,cin;
    output sum,cout;

    reg sum,cout;
    always @ (a or b or cin)
    begin
       sum <= a ^ b ^ cin;
       cout <= (a & b) | (a & cin) | (b & cin);
    end
endmodule
```

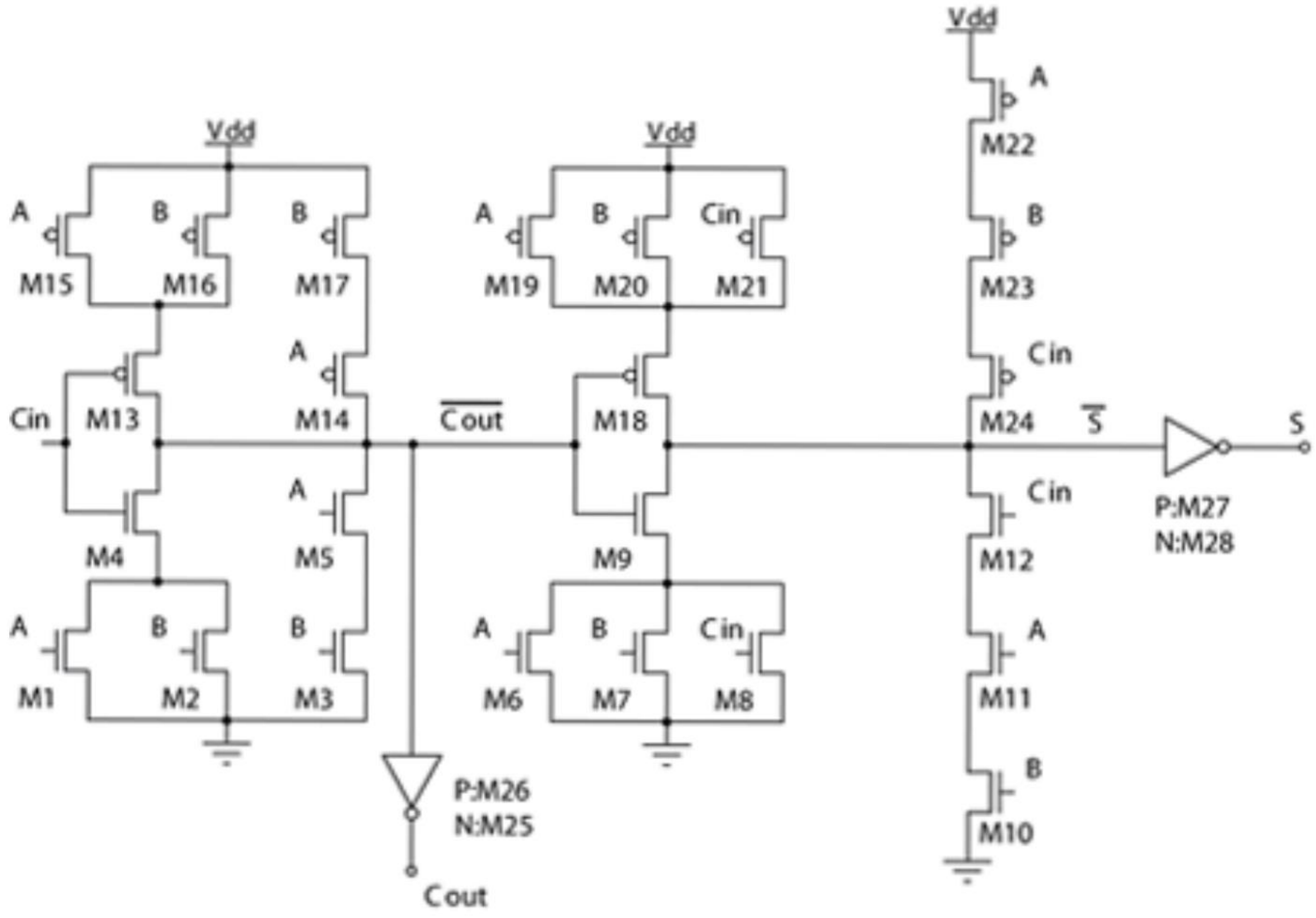
Logic Design

Full Adder Truth Table

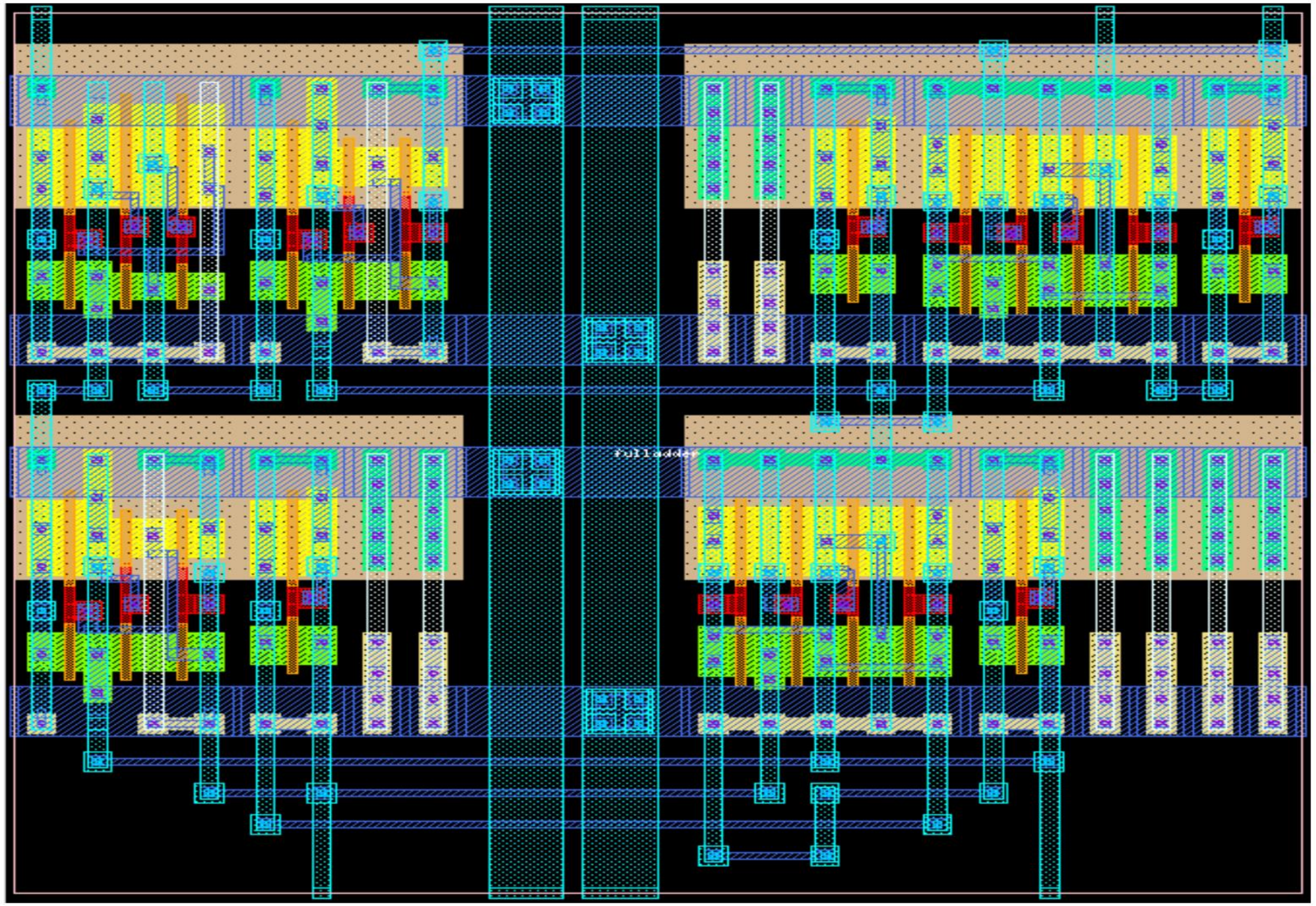
CARRY IN	input B	input A	CARRY OUT	SUM digit
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Transistor Schematic



Layout



VLSI Design Approaches

- Full custom
  - Design for performance-critical cells
  - Very expensive
- Standard cell
  - Faster
  - Performance is not as good as full custom
- Gate array
- Field Programmable Gate Array

VLSI Design Approaches

	Full Custom	Standard Cell	Gate Array	FPGA
Area	Compact	Moderate	Moderate	Large
Performance	High	Moderate	Moderate	Low

Production Volume:	**Mass Production Volume**	**Medium Production Volume**	**Medium Production Volume**	**Low Production Volume**
Complexity:	**High**			**Low**

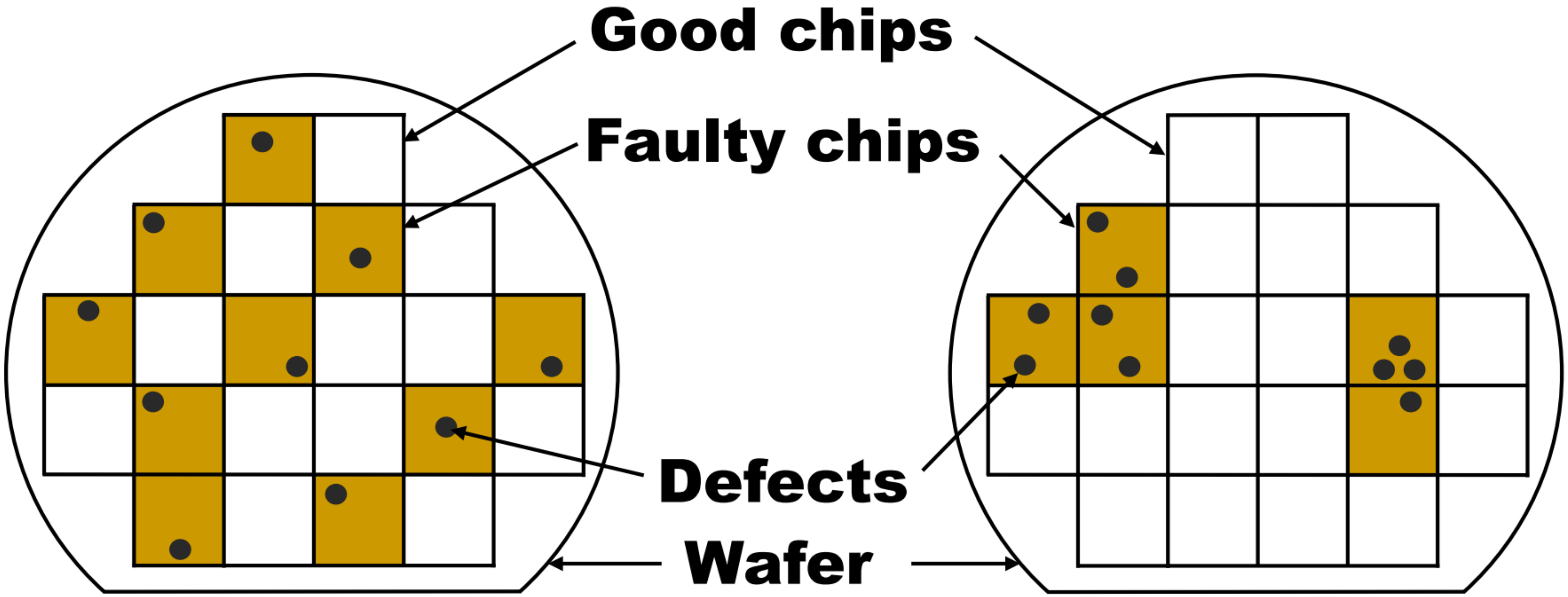
Chip Yield

- A manufacturing defect in the fabrication process causes electrically malfunctioning circuitry.
- A chip with no manufacturing defect is called a good chip.
  - The defective ones are called bad chips.
- Percentage of good chips produced in a manufacturing process is called the *yield*.
- Yield is denoted by symbol *Y*.

$$Y = \frac{\text{\# of good die}}{\text{\# total manufactured die}}$$

- How to separate bad chips from the good ones?

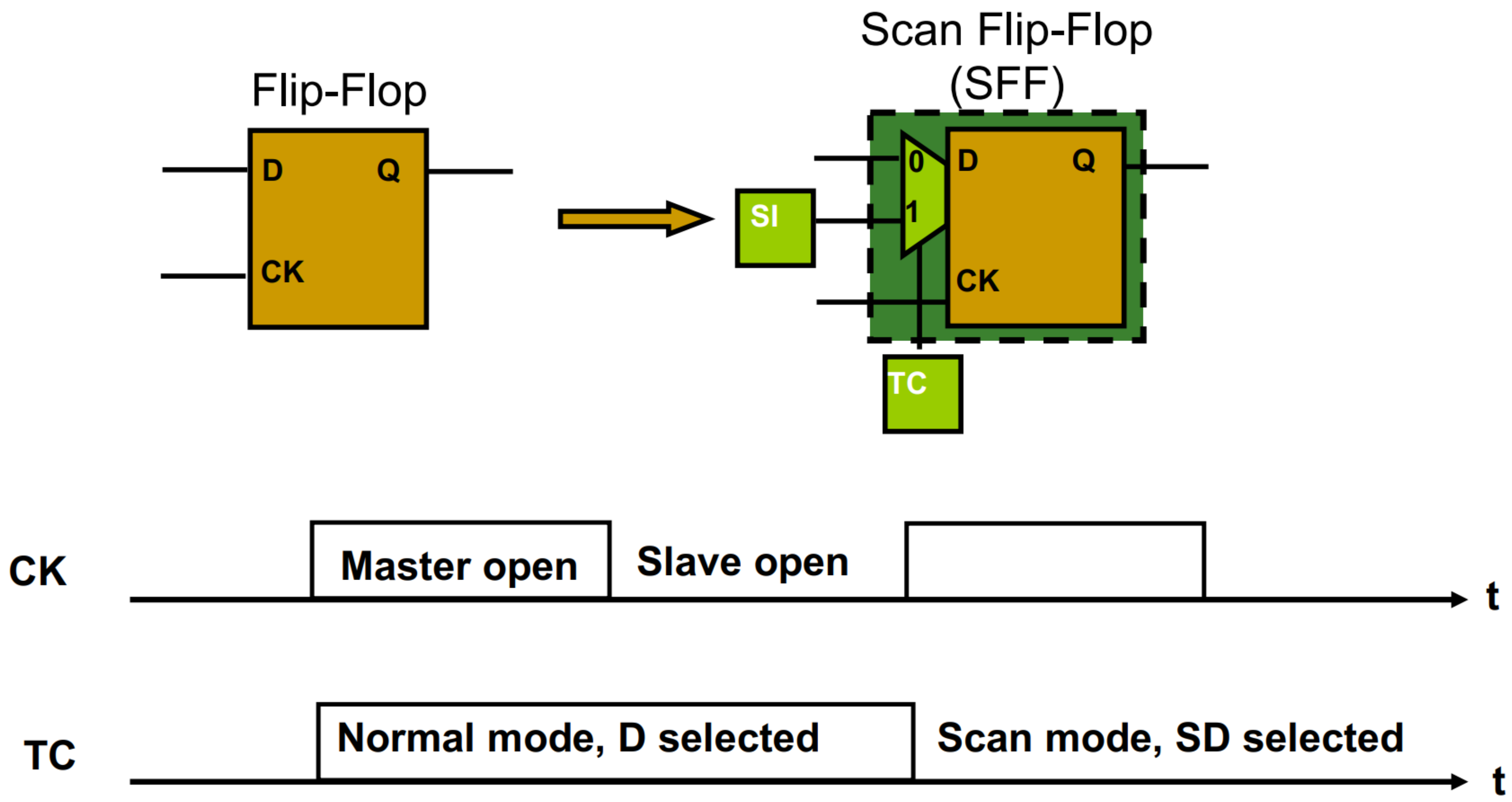
Chip Yield



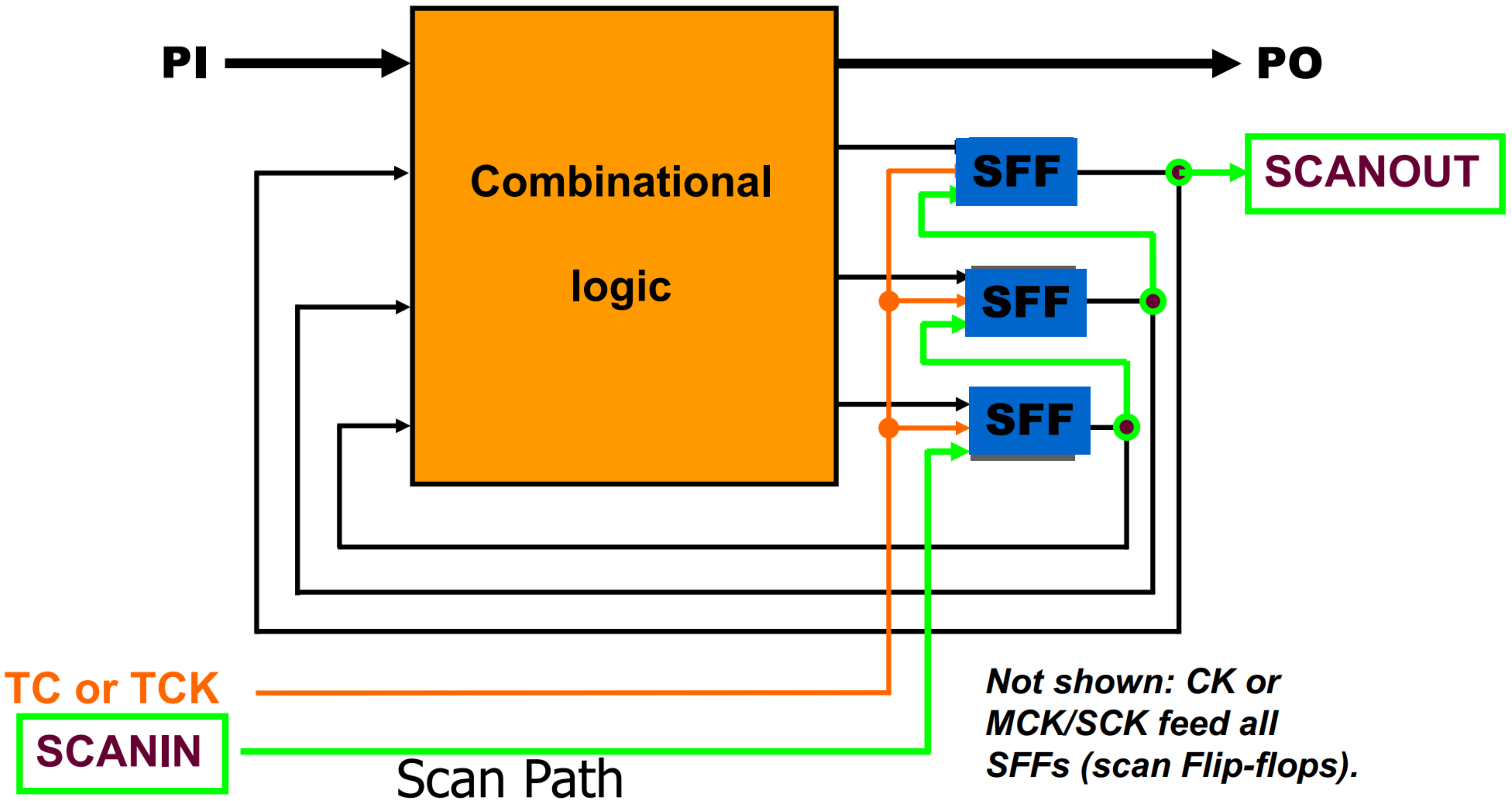
Unclustered defects
Wafer yield = 12/22 = 0.55

Clustered defects (VLSI)
Wafer yield = 17/22 = 0.77

Scan Chain

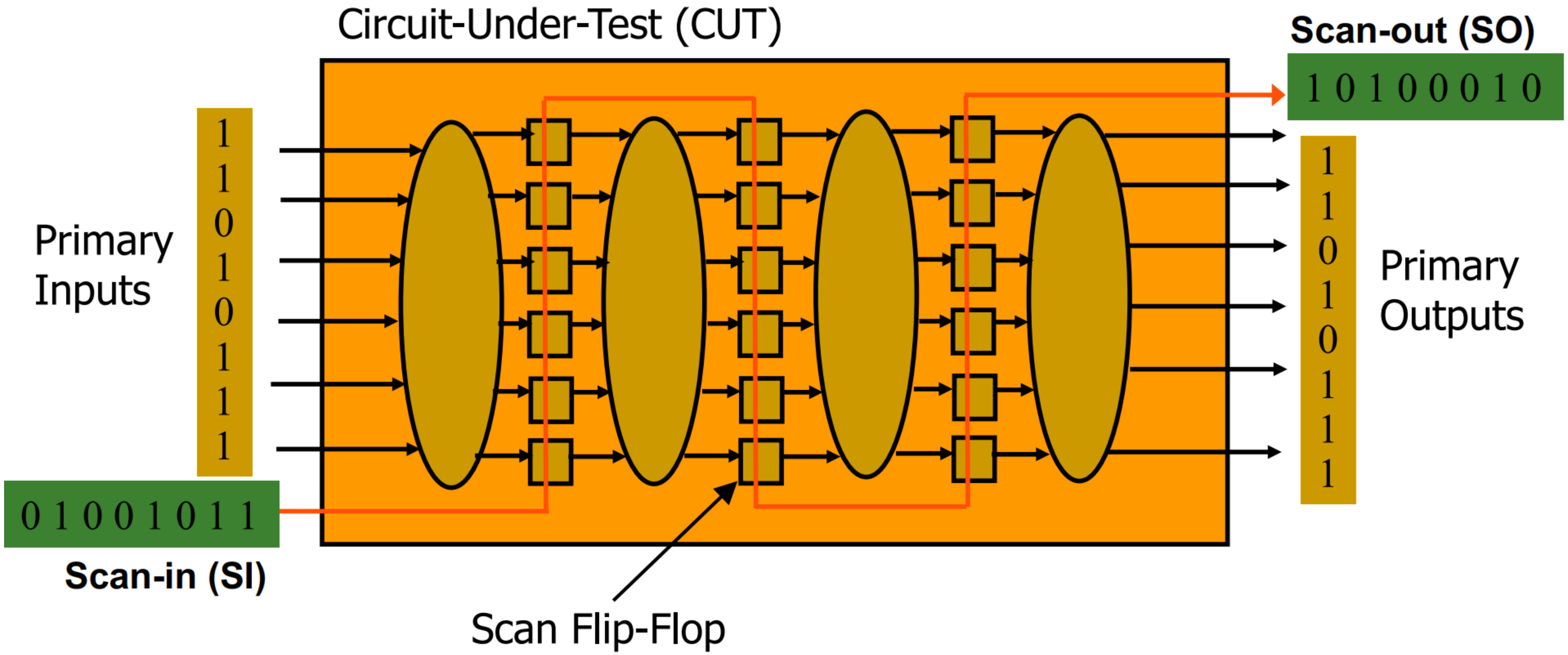

Flip-Flop
D
Q
CK
Scan Flip-Flop
(SFF)
SI
0
1
D
Q
CK
TC
CK
Master open
Slave open
t
TC
Normal mode, D selected
Scan mode, SD selected
t

Scan Chain



Scan Path
Also called Scan Chain

Scan Chain


Circuit-Under-Test (CUT)
Scan-out (SO)
1 0 1 0 0 0 1 0
Primary Inputs
1
1
0
1
0
1
1
1
Primary Outputs
1
1
0
1
0
1
1
1
0 1 0 0 1 0 1 1
Scan-in (SI)
Scan Flip-Flop